

FIG 1

The diagram shows a PLL circuit. A VCO (1) is connected to a divider (2) and an AGC (5). The divider (2) is connected to a control logic block (15) which receives FSK data. The control logic (15) is connected to a series of transistors (10, 11, 12, 13) which are part of a feedback loop. The feedback loop also includes transistors M1, M2, M3, M4, and M5. The output of the feedback loop is connected to a filter (8) and a reference voltage source (9). The output of the filter (8) is connected to the VCO (1) via a coupling capacitor (7). The output of the VCO (1) is also connected to the AGC (5) via a feedback line (3).

FIG 3

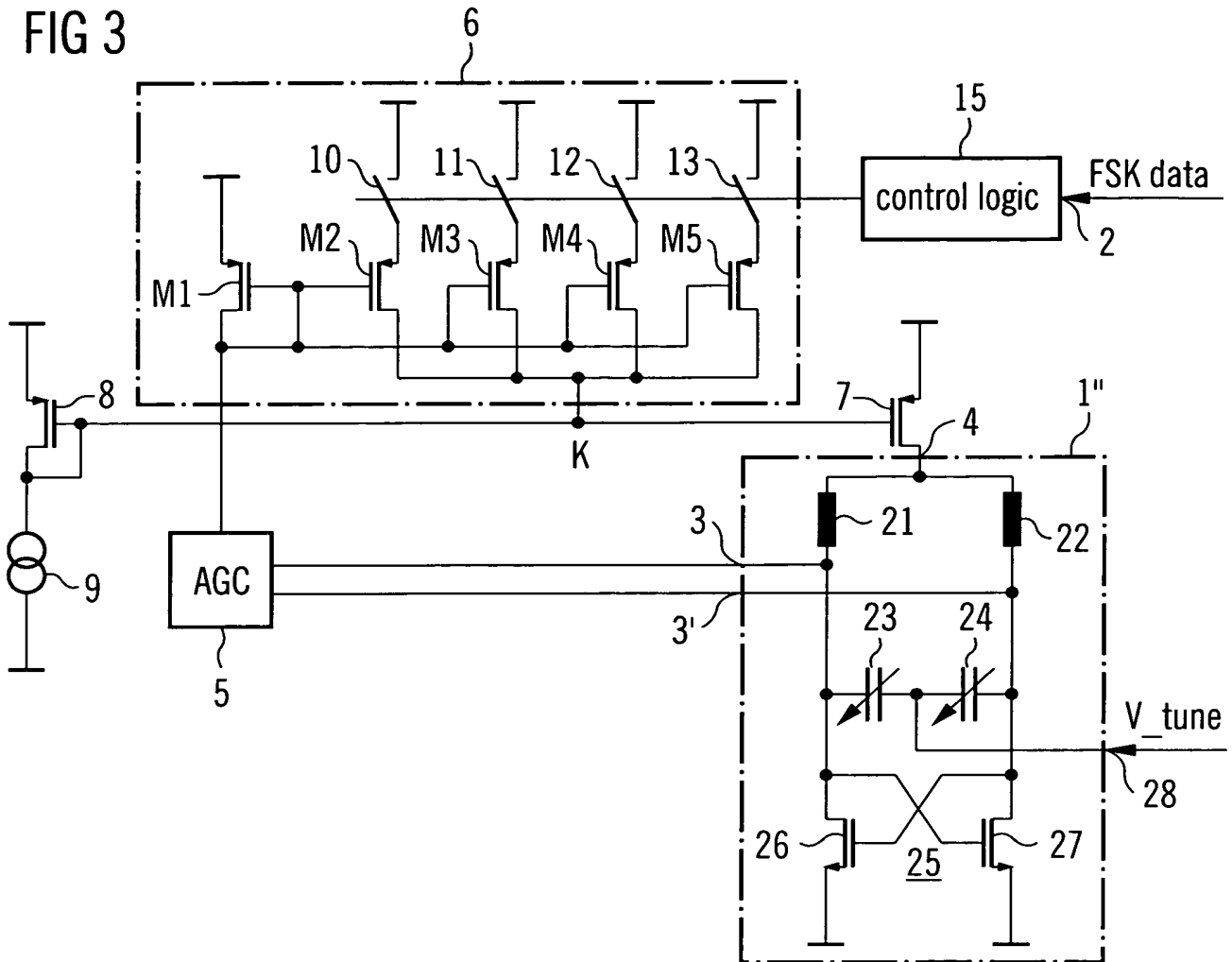


FIG 4

